

## Lithography-free fabrication of graphene devices

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We have developed a lithography-free, all-dry process for fabricating graphene devices using an ultrathin quartz filament as a shadow mask. This technique, which is free of the possible contamination of graphene during lithographic process, is simple to implement, versatile, and capable of achieving high throughput. We prepared devices for electrical transport as well as planar tunnel junction studies of  $n$ -layer graphene (nLG), with  $n=1,2,3$ , and higher using this technique. We observed possible weak localization behavior and an apparent reduction of density of states near the Fermi energy in nLG. © 2007 American Institute of Physics.

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There has been a flurry of recent work<sup>1,2</sup> on films of one-layer graphene (1LG), motivated by the pioneering work of Novoselov *et al.*<sup>3</sup> and Zhang *et al.*<sup>4</sup> Surprisingly, 1LG was found to host a two-dimensional electron gas with a band structure featuring zero effective mass.<sup>5</sup> Two types of unconventional integer quantum Hall effects were observed in 1LG (Refs. 1 and 2) and in two-layer graphene<sup>6</sup> devices. Theoretical calculation indicates that  $n$ -layer graphene (nLG) with  $n > 2$  is also interesting.<sup>5</sup>

The highest mobility reported for 1LG devices is around  $10\,000\text{ cm}^2/\text{V s}$  at high gate voltages,<sup>2</sup> which is remarkable. However, it may not be sufficiently high to allow the observation of certain physical phenomena, such as fractional quantum Hall effect. As a result, means to achieve higher mobility are needed. So far, all graphene devices reported in the literature were prepared by e-beam lithography. Multiple steps are required to pattern a device, including coating with organic materials, which may subject the graphene to possible contamination and add unwanted disorder to the device. In addition, the multiple steps of e-beam lithography device fabrication are expensive and time consuming. It is therefore desirable to pursue alternative graphene device fabrication. Using ultrathin quartz filaments as shadow masks, we have developed a method to fabricate graphene devices. This process is lithography-free, all dry, simple to implement, and scalable for large batch production. This process allows us to prepare several samples in a matter of hours. Devices fabricated were measured using a dc technique with a typical excitation current of  $1\ \mu\text{A}$  in a dip probe in which the sample was cooled by direct contact with <sup>4</sup>He liquid or gas.

Two methods have been used to create graphene samples—exfoliation either mechanically in air<sup>7</sup> or chemically in solutions,<sup>8</sup> and thermal decomposition of SiC.<sup>9</sup> Our nLG flakes were created by mechanical exfoliation in air from freshly cleaved highly oriented pyrolytic graphite (HOPG).<sup>10</sup> Heavily N-doped silicon with a 300-nm-thick thermally grown SiO<sub>2</sub> top layer was used as substrates, therefore all of our devices have a capacitance of  $1.15\text{ nF/cm}^2$

between the sample and gate, which will produce  $7 \times 10^{10}$  carriers/V. Thin graphene flakes were identified under an optical microscope with  $500\times$  magnification, as reported previously.<sup>1</sup> After inspecting a large number of exfoliated graphene flakes we concluded that the color and the faintness of the optical images of exfoliated graphene flakes fall into distinguishable patterns that can be organized into a “color-code” scheme for determining the thickness of nLG. This color-code scheme was correlated with atomic force microscopy (AFM) measurements in which the minimal height at the edge of the graphene flake was taken as the flake thickness. We also attempted to correlate our color-code scheme with the Raman spectroscopy measurements that provide information on the thickness of graphene flakes.<sup>11</sup>

An ultrathin quartz filament as thin as 200 nm in diameter, pulled from pure quartz melt, as described previously,<sup>12</sup> was placed onto the graphene flake of interest and used as a shadow mask. It was found that filaments around  $1\ \mu\text{m}$  in diameter could be manipulated most easily on a SiO<sub>2</sub> surface, but filaments as thin as  $0.2\ \mu\text{m}$  in diameter have been used. A film of Au was then evaporated, creating two electrodes serving as the source and drain [Figs. 1(a) and 1(b)]. We also fabricated planar tunnel junctions by evaporating a 2-nm-thick Al film at an angle ( $45^\circ$ ) that was allowed to oxidize in air to form an Al<sub>2</sub>O<sub>3</sub> tunnel barrier [Fig. 1(c)]. Two electrodes of Pb or Au were then deposited at a different angle, either vertical or  $135^\circ$ , to form a tunnel junction [Fig. 1(d)]. In both cases two fine Au wires were attached to each electrode using Ag epoxy to allow linear conductivity or tunneling measurements. Simultaneous measurements of both linear and Hall conductivities can be achieved by using a second filament to form a cross mask, which results in a van der Pauw probe.<sup>13</sup> It should be emphasized that we measure conductance in this work, while all data published so far on graphene devices have been on conductivity.

In Fig. 2(a), we show the conductance ( $G$ ) versus temperature ( $T$ ) for a 1LG device at three gate voltages ( $V_g$ ). Here  $G$  is calculated from sample resistance with the contact resistance ( $R_c$ ) included. It was reported previously<sup>4</sup> that the

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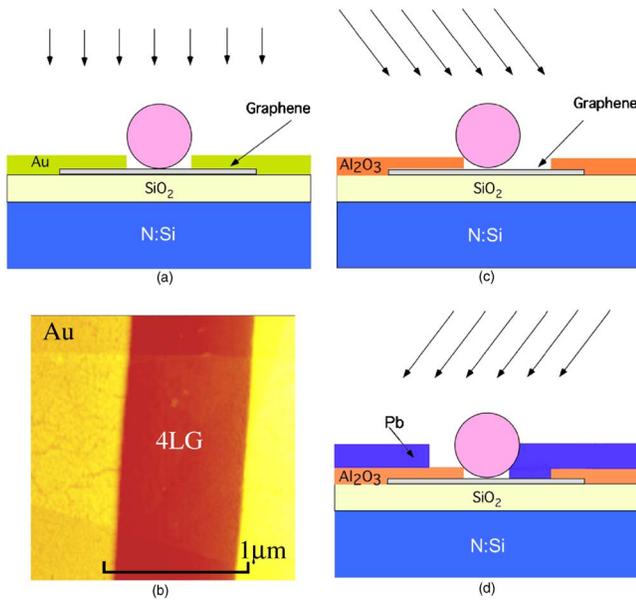


FIG. 1. (Color online) (a) Schematic for nLG device fabrication for transport measurement. An ultrathin quartz filament is used as a shadow mask. (b) AFM image of an actual four-layer graphene device. The graphene flake is visible. [(c)–(d)] Schematics for planar tunnel junction fabrication.

contact resistance ( $R_c$ ) between Au and graphene is small. The value of  $R_c$ , which could be inferred from examining the sample resistance at high  $V_g$  (providing an upper bound) or the linearity in the  $G$  vs  $V_g$  plot, was found to be much less than  $R$  for our nLG devices for small  $n$ . The hysteresis in  $G$  vs  $V_g$  is seen to be small [Fig. 2(b)], suggesting that few interface charge traps were present at or near the graphene-SiO<sub>2</sub> interface in this device, and all chemical dopants were immobile. Measurements over a wider range of gate voltages were not possible for this sample due to a large “leakage” current resulted possibly from an unintentional short. It is seen that this 1LG device follows a  $G \propto \ln(T)$  behavior for  $8 \text{ K} < T < 50 \text{ K}$ , consistent with weak localization in two dimensions (2Ds);<sup>14</sup> however, as we have not investigated the magnetoresistance for these samples there may be an alternative explanation for the observed behavior. Furthermore at high temperatures we observe that  $G \sim T^2$ , as shown in the inset; however, more measurements are needed for a full understanding of this behavior. It was reported previously that quantum interference responsible for weak localization

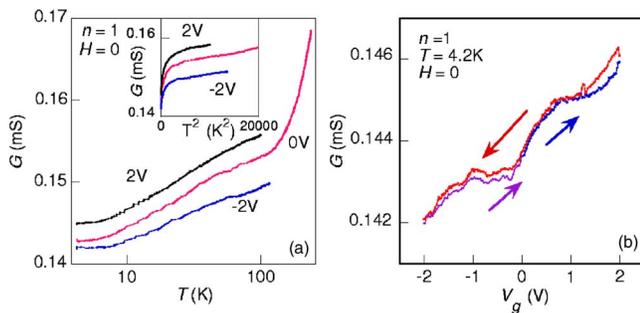


FIG. 2. (Color online) (a)  $G$  vs  $T$  for a 1LG device at three  $V_g$  values. Inset:  $G$  vs  $T^2$  plot of the same data. (b)  $G$  vs  $V_g$  loop. The arrows indicate how  $V_g$  was swept. Small hysteresis is seen. The range of  $V_g$  was limited in this device because of a leakage created by Ag epoxy spilled over to the edge of the doped Si substrate used as the back gate. The sample likely water doped as indicated by the asymmetry between positive and negative applied gate voltages.

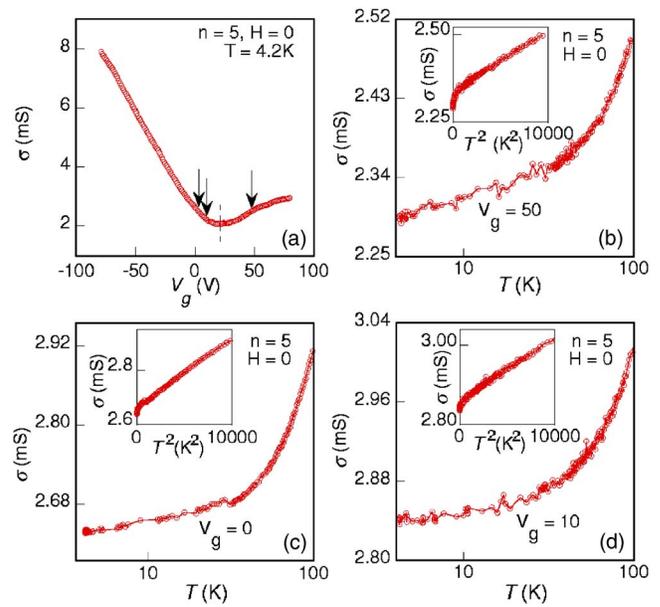


FIG. 3. (Color online) (a)  $\sigma$  vs  $V_g$  for a 5LG device. The arrows indicate the  $V_g$  at which  $\sigma$  vs  $T$  measurements were taken and the dash line shows the  $V_g$  at which  $\sigma$  reaches a minimum (25 V). [(b)–(d)]  $\sigma$  vs  $T$  in semilog plot at various  $V_g$  values as indicated; inset:  $\sigma$  vs  $T^2$ .

behavior could be suppressed in 1LG because of the local deformation of 1LG that results in random effective magnetic fields.<sup>15</sup> However, weak localization behavior was found at least in one sample.<sup>15</sup> It was emphasized that for 1LG, a minimum conductivity of  $4e^2/h$  was found at the Dirac point.<sup>1</sup> In other studies, however, conductivities very different from  $4e^2/h$  were also observed.<sup>2,4</sup> In fact, it is not clear whether conductance rather than conductivity should possess this quantum value. Interestingly, for this 1LG sample we measured, the conductance  $G$  appears to level off below 8 K at values close to  $4e^2/h$  ( $=0.155 \text{ mS}$ ). The implication of this observation is to be understood.

In Fig. 3(a),  $\sigma$  vs  $V_g$  of a gated five-layer graphene (5LG) device is shown. The asymmetric response suggests that the conduction and valence bands in a 5LG system have significant overlap, which leads to a density of states (DOS) that is asymmetric with respect to the Fermi energy  $E_F$ , consistent with theoretical expectations,<sup>5</sup> further asymmetry may be attributed to finite chemical doping likely due to water adsorption. For a device with a single type of carrier (electrons or holes),  $\mu = \sigma/n_c e$ , where  $\mu$  is the mobility,  $\sigma$  the conductivity,  $n_c$  the carrier density, and  $e$  the elemental charge. Because of the lack of Hall measurements, only the change of the carrier density by ramping  $V_g$  can be calculated from the capacitance. The mobility due to field effect is  $\mu_{\text{FE}} = (d/\epsilon_0 \epsilon) (\partial \sigma / \partial V_g)$ , where  $d$  is the thickness of the insulating barrier,  $\epsilon_0$  the permittivity of free space, and  $\epsilon$  the dielectric constant. For this 5LG device, the number of squares is approximately 1, making the conductance the same as conductivity. We obtain  $\mu_{\text{FE}} = 6700 \text{ cm}^2/\text{V s}$  for the holes at high (negative) gate voltages, which is not as high as that previously reported for 1LG devices. Refinement of our lithography-free technique will be needed to achieve higher mobility.

In this 2D 5LG device (1.8 nm thick), a temperature range in which  $\sigma$  shows  $\ln(T)$  behavior can be easily identified at  $V_g = 0$  and  $50 \text{ V}$  [Figs. 3(b) and 3(c)]. This  $\ln(T)$  be-

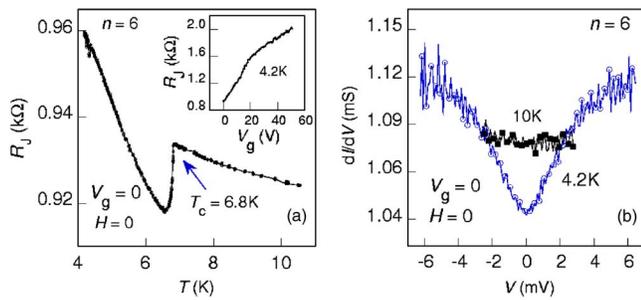


FIG. 4. (Color online) (a)  $R_J$  vs  $T$  for a Pb–Al<sub>2</sub>O<sub>3</sub>–6LG planar tunnel junction. Inset:  $R_J$  vs  $V_g$  at 4.2 K. (b)  $dI/dV$  vs  $V$  at two  $T_s$  as indicated. The drop in  $dI/dV$  near 2 meV at 4.2 K indicates the opening of an energy gap. Data on  $dI/dV$  at voltages higher than 2 meV at 10 K are not available.

havior may be associated with either quantum interference in the coherent backscattering or interaction effects for diffusive 2D carriers.<sup>14</sup> The observation of the  $\ln(T)$  behavior up to 50 K was surprising since at such high temperatures, the dephasing length should be very small. Interestingly,  $V_g=10$  V, close to the minimum in  $\sigma(V_g)$ ;  $\sigma$  is seen to follow the  $\ln(T)$  behavior less precisely [Fig. 3(d)]. This is reasonable—as the carrier density is lowered, the system becomes effectively more strongly disordered, leading eventually to deviation from the weak localization behavior. Interestingly, at higher temperatures where the  $\ln(T)$  dependence is absent,  $\sigma \sim T^2$  seems to describe the data the best, as shown in the insets of Figs. 3(b)–3(d). Further measurements, such as those on magnetoresistance, are needed to understand these observations.

In Fig. 4, we show results on a planar Pb–Al<sub>2</sub>O<sub>3</sub>–six-layer graphene (6LG) tunnel junction. Pb was chosen to be the top electrode primarily to test the fabrication process. As shown in Fig. 4(a), the junction resistance  $R_J(T)$  shows insulating behavior, suggesting that we do have a good tunnel barrier. A resistance drop was found at 6.8 K [Fig. 4(a)], the  $T_c$  of the Pb electrode, which is slightly lower than that of bulk Pb (7.2 K). At 4.2 K, below the  $T_c$  of the Pb electrode, the tunnel conductance, proportional to DOS, showed a drop around 2 meV, suggesting the opening of an energy gap [Fig. 4(b)]. The gap value was roughly twice of what is expected for Pb, most likely because two tunnel junc-

tions were formed in series, one with the designed Al<sub>2</sub>O<sub>3</sub> barrier and the other formed unintentionally because of the oxidation of Pb. There appears to be a suppression of DOS even at 10 K, above the  $T_c$  of Pb. Preliminary results obtained on tunnel junctions of Au–Al<sub>2</sub>O<sub>3</sub>–nLG suggest the same suppression.

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