Current-driven insulator–conductor transition and nonvolatile memory in chromium-doped $SrTiO_3$ single crystals

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Materials showing reversible resistive switching are attractive for today's semiconductor technology with its wide interest in nonvolatile random-access memories. In doped $SrTiO_3$ single crystals, we found a dc-current-induced reversible insulator–conductor transition with resistance changes of up to five orders of magnitude. This conducting state allows extremely reproducible switching between different impedance states by current pulses with a performance required for nonvolatile memories. The results indicate a type of charge-induced bulk electronic change as a prerequisite for the memory effect, scaling down to nanometer-range electrode sizes in thin films. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1377617]

Reversible resistive switching processes occurring in thin films of amorphous semiconductors,[1] polymers,[2–4] and ZnSe–Ge heterostructures[5] have engendered strong interest in these materials for application in nonvolatile memories. The memory behavior of oxides, based on current-induced bistable resistance effects or voltage-controlled negative resistance phenomena, as observed in compounds such as Nb_2O_5,[6] TiO_2,[7] Ta_2O_5,[8] and NiO,[9] has been studied in all-oxide thin-film heterostructures involving ferroelectrics[10] and simple metal–insulator–metal (MIM) structures.[11] The latter showed memory retention times exceeding 18 months. If bulk electronic mechanisms are considered to be of relevance for the memory effect, they involve charge-transfer processes including field and impact ionization of traps[8,12] and refilling by electron injection. To clarify whether the switching effect and the current transport across the insulator are mediated by microstructural defects in the thin films, we examined Cr-doped $SrTiO_3$ crystals as a model system.

We used (100)-oriented crystals doped with 0.2% Cr grown by flame fusion and thin films of $SrZrO_3$ doped with 0.2% Cr grown by pulsed-laser deposition.[11] Unless stated otherwise, the results are obtained from a crystal with a thickness of 10 μm. The initial resistance of the crystal was 1 GΩ up to 100 V at 4.5 K [Fig. 1(a)]. When sweeping the voltage to 200 V, the resistance suddenly drops, and a hysteretic current–voltage ($I-V$) characteristic (IVC) develops. Figure 1(b) displays the effect at 296 K. Subsequent stressing by pulsed or dc voltages of 50–90 V reduces the resistance further by orders of magnitude and creates a conductive state, which then enables memory switching between different impedance levels. The resistance of the conductive state is of the order of 500 Ω or 5 kΩ at 4.5 K and 200 Ω or 2 kΩ at 300 K for the low- (on) and high-impedance (off) state, respectively, and an electrode diameter of 0.8 mm (Au).

Typical IVCs of the conductive state after positive and negative pulses applied in current-control mode are shown in Fig. 1(c). The stability of the two levels was found to depend on the current density and the total charge passing through the crystal rather than on the amplitude of the voltage. A 1 ms pulse of 3.5 mA (''write'') sets the system to the on state, and a 1 ms pulse of -3.55 mA (''erase'') sets it back to the off state. The IVCs for two write and erase cycles were measured immediately and 5 h after application of the respective pulse, Fig. 1(c). The perfect overlay demonstrates a superb reproducibility. The resistance change is ''read'' by applying a 1 ms pulse of -0.5 V in voltage-control mode [inset in Fig. 1(c)]. The data read immediately and 24 h after the write/erase pulses show the perfect memory retention.

Between 4.5 and 10 K, the IVCs remain unchanged, whereas at higher temperatures the resistance is increased with the two states having different temperature coefficients, Fig. 1(d). However, the temperature (T) dependence of a current (I) in the off or on state as recorded during $I-T$ scans exhibits a more complex behavior. Nonlinear changes during heating/cooling between 4.2 and 300 K originate from carrier trapping or emission, as known from thermally stimulated current spectroscopy.[13] Even at low voltages (1 mV) does the on state tend to change into the off state during T cycles. At extremely low scan speeds, the latter can even revert to the insulating state. This transition, accompanied by carrier emission, and the method of creating a conductive state by exposing an insulating crystal to high voltages or high-current densities suggest that this conductive state originates from an excess of injected carriers. If so, creation of this state should also be possible by a low voltage and small currents. This was verified in thin-film experiments. The application of $+0.4$ V for a long period (current density $\sim$20 mA/cm^2) increases the resistance of a $SrZrO_3$:Cr thin film by three orders of magnitude, Fig. 2(a), with the corresponding IVCs shown in Fig. 2(b). Reversing I at -0.4 V for a long time brings the system back to the conductive state, a requirement for memory switching between two or several levels.

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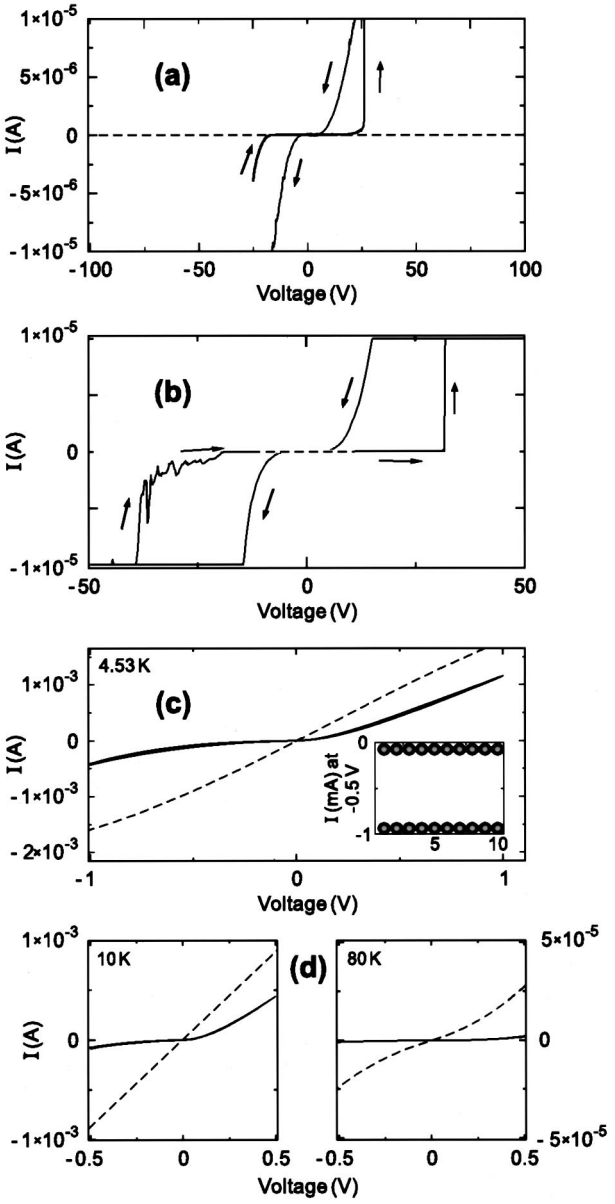

FIG. 1. IVCs recorded on a $SrTiO_3$:Cr single crystal (thickness, 10 μm), showing the change from an insulating (dashed line) to a conducting state (solid line) by current stress at (a) 4.5 K and (b) 296 K. IVCs of the on state (solid line) and off state (dashed line) at (c) 4.53 K and (d) 10 and 80 K. In (c), the curves for two write and erase cycles (four records per state) are measured immediately and 5 h after the respective pulses. Inset shows ten readouts of the corresponding states of the memory recorded immediately after (black circles) the write or erase pulses and 24 h later (shaded circles).

Once the conductive state is established, crystals display characteristics similar to the thin films,[11] underlining the potential of these oxides as nonvolatile random-access memories (RAMs). The record of the on and off states for hundreds of write–read–erase cycles shows a remarkable stability [Fig. 3(a)] with no change of the readout signal after more than 10^5 readouts [Fig. 3(a), inset]. A similar stability is confirmed in a $SrTiO_3$:Cr crystal with a greater thickness, i.e., 0.5 mm. As apparent in thin-film experiments,[11] write pulses of different current amplitudes can create multiple on states. At 4.5 K we could write and erase up to six states by 1 ms pulses of 1.5, 2.2, 2.5, 2.7, 3, 3.5, and −3.55 mA, Fig. 3(b). To demonstrate the stability of the different levels, each write or erase pulse was followed by 10^3 readout pulses at −0.5 V.

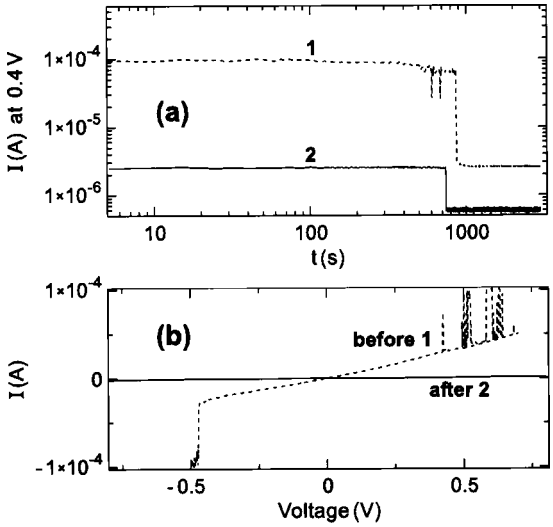

FIG. 2. (a) Two successively measured $I-t$ characteristics of a $SrZrO_3$:Cr film (100 nm) with a $SrRuO_3$ bottom electrode and a 0.5 mm^2 Au top electrode. (b) IVC before (1) and after (2) the $I-t$ measurements (at RT).

Multiple states, not restricted to low T but also obtained at 300 K, are reproducibly controlled over 10^3 write/erase cycles with a total of 10^4 read pulses.

The scalability of this remarkable performance will be of great relevance for the technological realization as nonvolatile RAM. We have demonstrated well-defined switching and memory behavior in $SrZrO_3$:Cr films (Fig. 4) with electrode

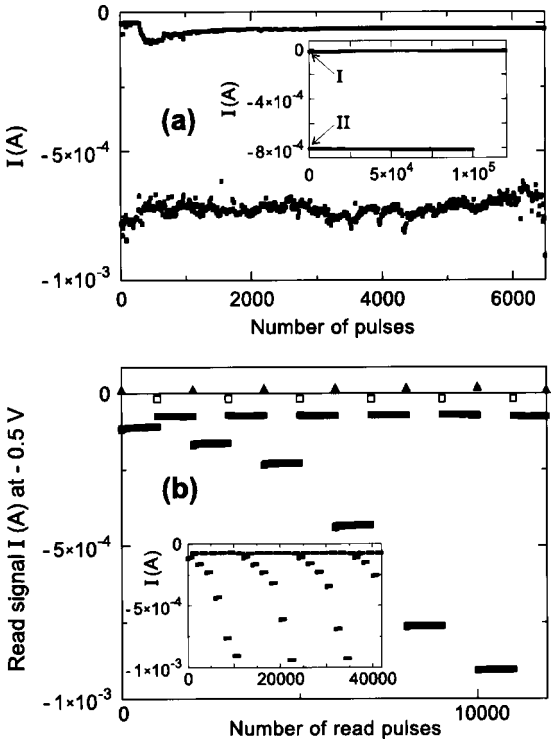

FIG. 3. (a) Stability of the switching characteristics of a single crystal during more than 500 write/erase cycles at 296 K. After each write (+7.7 mA) or erase (−8 mA) pulse, five readout pulses (−0.3 V) are applied. Inset shows the stability of 10^5 readouts of an off state (I) and on state (II) at 296 K following a single write or erase pulse. (b) Multiple on states obtained at 4.5 K after write pulses (▲) with different current amplitudes of 1.5, 2.2, 2.5, 2.7, 3.0, and 3.5 mA and erase pulses (□) with a fixed amplitude of −3.55 mA. The ▲ and □ pulses are shown only schematically on top. Each pulse is followed by 1000 readouts (−0.5 V). Inset shows readout currents for 3.5 write–erase cycles with a total of 42 000 pulses.

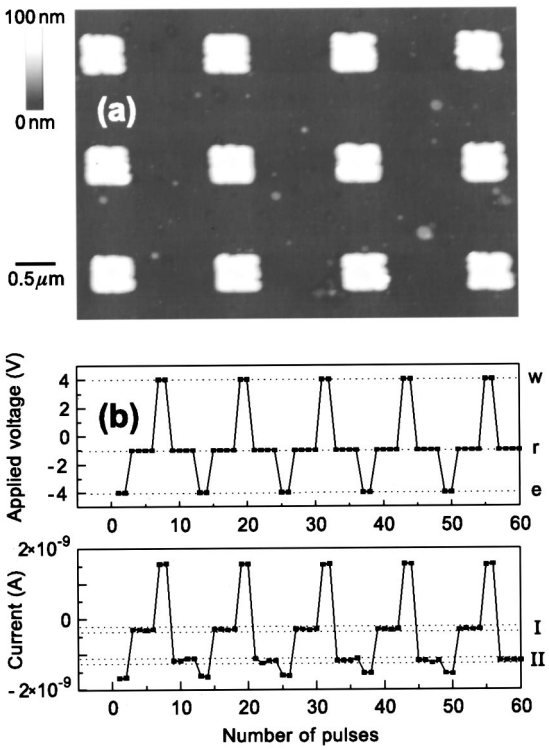

FIG. 4. (a) AFM image of Ti/Pt electrodes ($500\times500\,nm^2$) on a 3-nm-thick $SrZrO_3$:Cr film (defined by electron-beam lithography). (b) Switching properties (at RT) on pads addressed by an AFM with write (w), erase (e), and read (r) by 1 ms pulses. (I) labels the on state and (II) the off state.

(Ti/Pt) sizes down to $100\times100\,nm^2$. These contacts were addressed via the conducting tip of an atomic-force microscope (AFM).[14] Currents scaled linearly with the electrode area as estimated from experiments on mm-scale electrodes.

The results on crystals provide insight into the processes leading to the complex behavior related to the memory effect. The existence of a high initial resistance up to 100 V confirms that the bulk, and not the interface, determines the current flow across the insulator and that the transition to the conducting state originates from a change in the bulk property. As this transition and well-defined memory switching with long-time stability occur in single crystals having 0.01–0.5 mm electrode separation, as well as in thin films with submicron electrodes, a significant contribution to this phenomenon by defects like grain boundaries can be excluded. The stressing process required to create the conducting state, the emission of trapped carriers, and giant conductance changes during $I-T$ scans indicate that this state is created by carrier trapping in the bulk.[15,16] Likewise, the current conduction in SiO_2 could be explained by the injected-carrier-induced change of the local electronic structure at impurities,[17] suggesting a similar mechanism in perovskite oxides. This is in contrast to thermally activated processes for degradation and recovery of the bulk resistance[18] based on oxygen–vacancy migration[19] because the conducting state can even be obtained through stressing at 4 K. In addition, various types of (orbital) ordering occurring in perovskites, such as ion ordering in ferro- and antiferroelectrics or the spin-charge ordering in $(La, Sr)MnO_3$ (Ref. 20) and high-T_C superconductors,[21] suggest that changes of the electronic structure, or a local variation of the oxygen polyhedra, or a combination of both, can be induced by carrier injection. Indeed, the destruction of charge order in $(La, Sr)MnO_3$ by current injection[22] resulted in an enhanced conductance.

When in $SrTiO_3$ crystals the bulk is sufficiently conductive, the interface, i.e., the Schottky barrier, starts to control the current, as confirmed by the double Schottky-like IVCs [Figs. 1(c) and 1(d)] and the typical turn-on voltage of 1 V at 4.5 K. As apparent from the IVCs of the off states in Figs. 1(c) and 1(d), the stressing creates an asymmetry between the two barriers of the otherwise symmetric MIM structure. The switching can then be attributed to carrier-injection-induced degradation and carrier-emission-induced recovery of the Schottky barrier that is more resistive than the other. The long-time memory retention probably needs an explanation based on the specific valence properties of the perovskites. This first demonstration of the memory effect in single crystals allows the physics behind the effect to be studied by various methods of solid-state physics. Electron-spin resonance and optical absorption, used to determine the various electronic levels of transition-metal impurities in $SrTiO_3$,[23–25] and photoconductivity experiments, which revealed memory behavior at low T.[26]

In conclusion, our results introduce a reversible insulator–conductor transition, which implies that in the analysis of insulating films along traditional lines, an interpretation of the leakage–current phenomenon, where an apparent breakdown can be electrically restored, is appropriate.

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