Nanometer-scale two-terminal semiconductor memory operating at room temperature

A. M. Song[a] and M. Missous
School of Electrical and Electronic Engineering, University of Manchester, Manchester M60 1QD, United Kingdom

P. Omling, I. Maximov, W. Seifert, and L. Samuelson
Solid State Physics and Nanometer Consortium, Lund University, S-221 00 Lund, Sweden

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Based on a nanometer-scale semiconductor channel with an intentionally broken geometric symmetry, we have realized a type of memory device that consists of only two terminals, rather than the minimum of three terminals in conventional semiconductor memories. The charge retention time is at least 10 h at cryogenic temperatures and a few minutes at room temperature. Furthermore, the simplicity of the design allows the active part of the devices to be made in a single nanolithography step which, along with the planar structure of the device, provides promising possibilities for a high integration density. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1852711]

As semiconductor device dimensions rapidly reduce to the nanometer scale, physical phenomena and effects arise, such as single-electron charging effect,[1–3] ballistic electron transport,[4–6] and quantized conductance.[7,8] These effects have in recent years allowed researchers to generate ideas to design and fabricate electronic devices that operate with different but often very simple working principles. So far, most of the studies on nanoelectronic devices have focused on electron transport inside the bulk of the active region of the devices. Much less attention has been given to the surface of these nanostructures. As the feature size of electronic devices reduces, the surface-to-volume ratio increases dramatically. The properties of the top and/or sidewall surfaces, such as composition, roughness, charge states, and Fermi-level pinning, before and after surface treatments, often overwhelmingly determine electron transport in these structures, and would therefore significantly influence or even govern the device characteristics. Such phenomena are in strong contrast to conventional semiconductor devices, and may, in many cases, cause undesirable effects. For example, a single-electron transistor (SET) was found to be extremely sensitive to fluctuating background charges. A single charged impurity in the close vicinity of a SET can significantly influence its operation, which is possibly the most serious problem to integrate SETs for practical applications.[9–11] Investigations to find ways of mastering surfaces, i.e., allowing a high degree of control of the surface physical and chemical properties, become increasingly demanding and crucial.

Alternatively, rather than regarding surfaces and/or interfaces as a problem to avoid or eliminate, it is possible that the surface and/or interface of a nanostructure may be utilized to serve as a component useful for device applications, and may even become an "active" region of a nanometer-scale device. By such functionalization of the surfaces of nanostructures, a number of routes could be opened to allow realization of a series of device concepts.

In this work, we demonstrate a type of nanometer-scale memory device by utilizing the high surface-to-volume ratio of a narrow semiconductor channel. The device structure is based on the recently reported self-switching diode (SSD), in which diodelike current-voltage (I-V) characteristics were realized by tailoring the boundary of a narrow semiconductor channel to break its symmetry.[12] Unlike a diode, neither doping junction nor tunneling barrier is needed in a SSD for its nonlinear property. The threshold voltage can also be widely tuned by simply changing the channel width. Recently, operations of SSDs in the terahertz (THz) regime have been envisaged,[13] signifying that such devices are relevant for future high-frequency electronics. Here, we demonstrate that the SSD structure can also be used as a memory device that operates at room temperature. The working principle is entirely different from that of conventional semiconductor memories. Unlike a semiconductor dynamic random access memory (DRAM), the device has only two terminals and the structure is planar, showing promising possibilities for a high integration density for this type of memory. The charge retention time ranges from at least 10 h at cryogenic temperatures to a few minutes at room temperature, which is orders of magnitude longer than standard DRAMs. We also present a model for this self-switching memory (SSM) device based on the surface functionalization of the narrow semiconductor channel.

The SSMs were fabricated using a modulation-doped $In_{0.75}Ga_{0.25}As/InP$ quantum-well wafer grown by metalorganic vapor phase epitaxy. The heterostructure contains a two-dimensional electron gas (2DEG) in a quantum well 40 nm below the surface. The sheet carrier density and mobility at a temperature of $T=4.2$ K are 4.5×10^{15} m^{-2} and 45 m^2/V s, respectively. At room temperature, the figures are 4.7×10^{15} m^{-2} and 1.2 m^2/V s, respectively. Like the fabrication of SSDs, producing SSMs requires only one step of nanolithography, rather than multiple-mask alignments. Figure 1 is an atomic force micrograph of a typical self-switching memory, in which the dark areas (two lines) were etched through the 2DEG layer and became insulating. Details of the fabrication of the insulating grooves have already been reported.[12] The continuation of the trenches to the device boundary breaks the symmetry, resulting in a diodelike nonlinear I-V characteristic for the current flow in the narrow

[a]Author to whom correspondence should be addressed; electronic mail: a.song@manchester.ac.uk

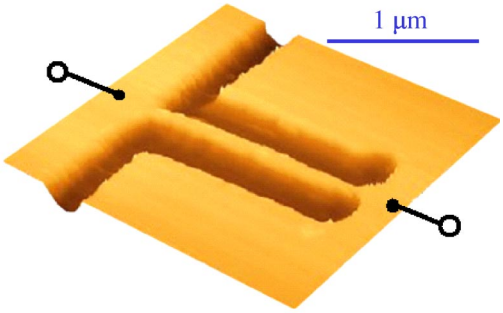

FIG. 1. (Color online) An atomic force micrograph of a typical SSM device consisting of two etched trenches. Also schematically shown are the two bias contacts.

channel between the etched grooves. This was presented in detail in Ref. 12, and is also shown by the dashed line between −0.8 V to +0.8 V here in Fig. 2(a), which was measured at $T=24$ K.

Within ±0.8 V the *I-V* curve of the SSM is independent of the voltage sweep direction, however a pronounced hysteresis effect emerged when the applied negative voltage passed beyond a threshold of about −0.9 V, where a current breakdown was observed. Once the breakdown happened, sweeping voltage backward resulted in a very different *I-V* characteristic, as shown by the solid line in Fig. 2(a). An overall larger conductance of the solid curve is clearly evident, particularly under the reverse bias condition. If, however, the applied voltage is reduced from, e.g., +1 V, the current would recover and follow the dashed curve in Fig. 2(a). This thus dramatically differs from the breakdown of a normal diode, where the *I-V* curve is independent of the voltage sweep direction, unless the applied bias is so strong that the device is destroyed.

Such a hysteresis effect can be utilized for memory operations. At −0.5 V, for example, the current is either zero (may be regarded as memory state "0") or about −2.5 μA (defined as memory state "1"). To demonstrate this, we applied voltage pulses to the device, and monitored the current. In Fig. 2(b), we started with a pulse of −0.5 V to detect the current memory state, and the nonzero current indicated that the device was at memory state 1. Another pulse after about 1 min still yielded a nonzero current, showing that the device could maintain its memory state. Further experiments demonstrated that the device could hold its memory state at least overnight (the longest time that was tested) at 24 K. To

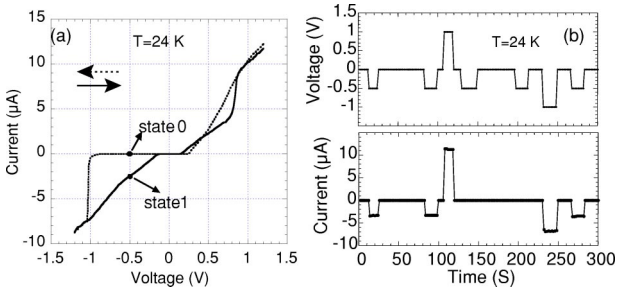

FIG. 2. (a) *I-V* characteristics of a typical SSM measured at $T=24$ *K*. (b) Experimental results of the memory effect, performed with test pulses at −0.5 V, and state-switching voltages of ±1 V. After each pulse of +1 V, the current remains zero during test pulses of −0.5 V, corresponding to the memory state of 0. After each pulse of −1 V, the current becomes nonzero during test pulses, corresponding to the memory state of 1.

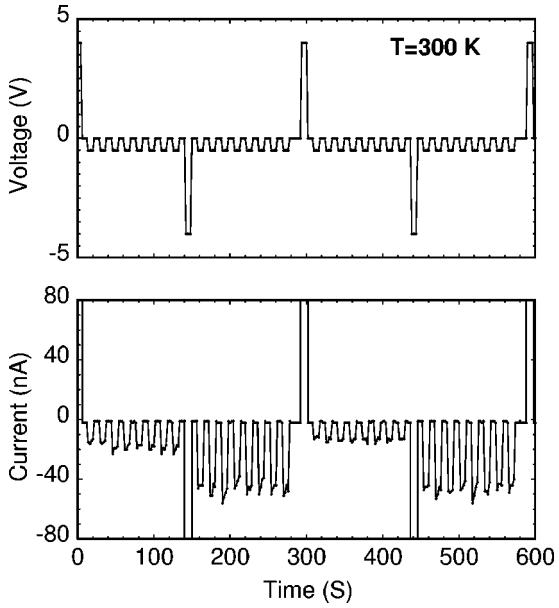

FIG. 3. Experimental results of the memory effect at room temperature, performed with test pulses of −0.5 V, and state-switching voltages of ±4 V.

switch from state 1 to state 0, we applied a positive pulse of 1 V, and the subsequent test pulse of −0.5 V indeed yielded zero current. The device also held the memory state 0, as is evident by another −0.5 V pulse shown in Fig. 2(b). The ability for the device to switch from memory state 0 to state 1 was demonstrated by applying a −1 V pulse, after which the device produced a nonzero current when −0.5 V was applied, as illustrated in Fig. 2(b). Note that here the long switching pulses of 1 and −1 V were used for clarity. The hysteresis effect was also observed by applying triangular waves up to 10 kHz (the limit of our setup) to the device, meaning that the memory switching time is below or at least in the order of μs.

This memory effect can be observed up to room temperature. Figure 3 shows the results obtained with test pulses at −0.5 V, and state-switching voltages of ±4 V. At $T=300$ K, the memory state 0 no longer corresponds to zero current (or conductance), but is still distinctively lower than at memory state 1. From the result, the memory holding time was found to be in the order of minutes, which is orders of magnitude longer than that of a typical semiconductor DRAM. Although this is not yet comparable to flash memories, based on our model, presented below, we expect that further optimizations of material composition, device design, side-wall coating, and surface treatment, could significantly increase the charge retention time.

Apart from the long memory holding time, the two-terminal nature of the SSM may also simplify the architecture of memory chips. Moreover, only one step of high-resolution lithography was needed, making it possible to use nanoimprint techniques to produce large SSM chips. This may significantly reduce both the cost and difficulty of modern lithography processes, which currently require multiple steps of mask alignment with increasingly challenging alignment precisions of below ~20 nm needed for sub-100 nm features.

The self-switching memory is based on a completely different working principle from a conventional semiconductor memory. To understand the memory effect, we propose the

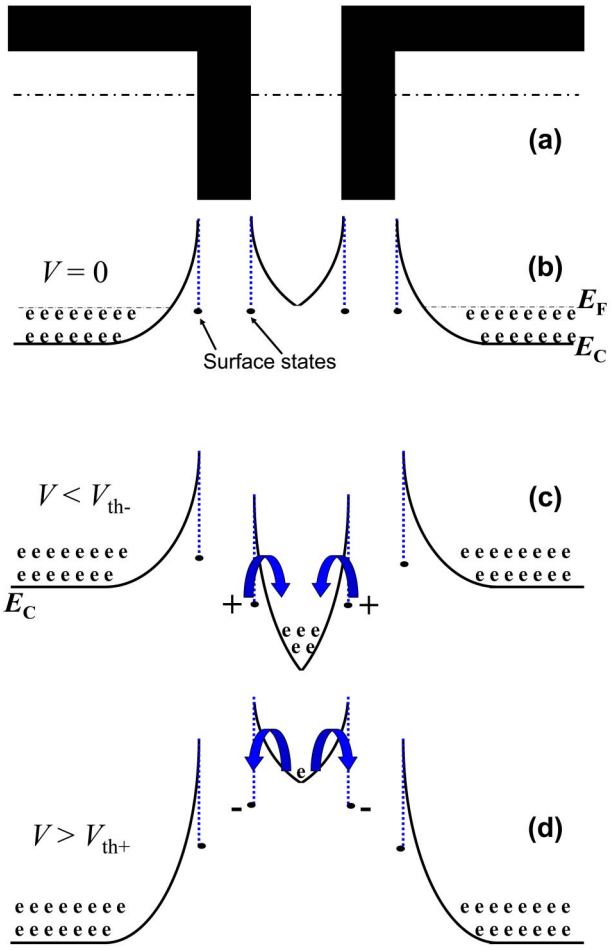

FIG. 4. (Color online) (a) A sketch of an SSM. (b) The conduction-band profile along the dashed line in (a). (c) When the applied bias is beyond the negative threshold voltage, V_{th-}, the surface states will be discharged by charge transfer into the channel. The opposite process happens if the applied bias is beyond the positive threshold, V_{th+} (d).

following model. We first notice that after the breakdown at about -1 V, the *I-V* curve (solid line) in Fig. 2(a) became rather symmetric around the origin, almost completely losing the diodelike asymmetric *I-V* characteristic. This indicates that the self-switching effect as illustrated in Fig. 1 in Ref. 12 has been largely screened. Such a screening effect can only be caused by charge migrations and storage within the 2DEG plane, which appears to be possible only at the side walls of the etched trenches. Figure 4(b) illustrates the conduction-band profile along the dashed line in Fig. 4(a). As is typical in III-V semiconductor materials, the conduction band bends up close to the side walls of the etched trenches, due to the charging of electrons into the surface states. The surface states are generally close to the middle of the band gap with a narrow energy distribution. At zero bias, the surface states are in equilibrium with the 2DEG, and the Fermi energy, E_F, is below the conduction-band bottom in the channel because the channel is completely depleted. When the applied bias is beyond the negative threshold voltage, V_{th-}, the conduction band in the channel lowers so much that the surface states are significantly discharged by electron transfer into the channel, either by tunneling or thermal excitation, depending on the temperature and potential profile. This is shown in Fig. 4(c). After the charge transfer, the side wall surface becomes less negative (or more positive) and this field effect enhances the overall conductance of the device, in agreement with the experimental result (solid line) in Fig. 2(a). Because of the potential barrier between the surface states and the channel, such charge transfer only becomes pronounced when the bias is beyond a certain threshold voltage to reduce the effective potential barrier width, as shown in Fig. 4(c). Note, however, that even if the device is biased slightly below the threshold, a significant number of electrons can also be discharged after waiting for a longer time and the same effect should occur, which was confirmed in our experiment (details not shown here). Once the side wall surfaces are discharged, a large positive bias will induce the opposite charge transfer process, as illustrated in Fig. 4(d), which explains how the device recovers after the application of a large positive voltage. The above picture has qualitatively explained our experimental observations. A complete model for the memory effect would require numerical simulations to study the detailed surface states and potential profiles, which is beyond the scope of this letter but would lead to significant optimizations of the device performance.

We have also observed memory effects in SSMs fabricated from InGaAs/InAlAs wafers (details to be reported elsewhere). Like SSDs, since the device operation does not rely on the ballistic electron transport, we expect that SSMs can also be produced using silicon materials by advanced complementary metal oxide semiconductor (CMOS) technologies. Actually, the device performance may be significantly improved by deposition of suitable materials into the trenches of a SSM, which would provide the freedom to engineer desirable surface/interface states and even the possibility of creating nonvolatile memories. Further explorations of the functionalization of surfaces could perhaps also lead to other concepts for nanodevice designs.

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