Nanometer-scale switches using copper sulfide

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We describe a nanometer-scale switch that uses a copper sulfide film and demonstrate its performance. The switch consists of a copper sulfide film, which is a chalcogenide semiconductor, sandwiched between copper and metal electrodes. Applying a positive or negative voltage to the metal electrode can repeatedly switch its conductance in under 100 μs. Each state can persist without a power supply for months, demonstrating the feasibility of nonvolatile memory with its nanometer scale. While biasing voltages, copper ions can migrate in copper sulfide film and can play an important role in switching. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1572964]

Nanoscale electronic devices such as molecular[1–3] or atomic devices[4–6] have been extensively investigated to overcome the limitations in silicon-based microelectronics. Recently, a conductance switching phenomena caused by the creation or annihilation of nanoscale metallic wire have been observed on the surface of Ag_2S/Ag film using a scanning tunneling microscope (STM).[6] The Pt tip of STM is set at a distance of a few nanometers from Ag_2S/Ag film, which is a mixed Ag-ionic/electronic conductor. When a negative voltage is applied to the tip, Ag ions on the surface are neutralized and a metal bridge in its nanometer scale is formed in the gap between the tip and the Ag_2S film.[7] When a positive voltage is applied, the bridge dissolves into the film and the conductance decreases. To integrate large numbers of these Ag_2S switches, it is essential to fabricate nanometer gaps uniformly.

Here, we demonstrate that the conductance of the mixed ionic/electronic conductor can also be switched without it having a nanometer gap. The mixed conductor sandwiched between two metals shows reproducible switching in its conductance with a memory effect. Instead of Ag_2S, we use Cu_2S, which is a mixed Cu-ionic/electronic conductor and is suitable for device application. We show that the device can operate at low voltages (<0.3 V) and that the size can be scaled down to a nanometer regime.

The device structure is depicted in Fig. 1(a). The top layer is a Au/Pt/Ti electrode, which electrically contacts with the Cu_2S/Cu film through a hole in the insulating layer. The fabrication sequence is as follows. A 120-nm-thick Cu film on Si_2O/Si is sulfidized using anodic polarization. The Cu film is immersed into a 0.025 M Na_2S solution. A positive voltage is biased to the film while grounding the immersed Au electrode. As the voltage is biased, sulfide ions are absorbed on the surface of the film, and then the surface is sulfidized electrochemically. The ionic current between two electrodes can be monitored during the polarization. Molar ratio between Cu and S in the sufidized film is estimated to be 2:1 using Rutherford backscattering. At room temperature, copper sulfide can form five stable phases: covellite CuS, anilite $Cu_{1.75}S$, digenite $Cu_{1.8}S$, djurleite $Cu_{1.95}S$, and chalcocite Cu_2S.[8] We deduce that the phase of the fabricated film is a chalcocite Cu_2S, which is a Cu-ionic conductor and also a p-type semiconductor.[9] After sulfidization, an insulating layer with a hole is made from a chloromethylated calixarene film, which is an electron beam (EB) negative resist, using EB lithography.[10] The diameter of the hole ranges from 0.03 to 0.3 μm. The hole defines the contact area of the Cu_2S film with the top electrode. Finally, the top electrode of the Au/Pt/Ti is formed. Figure 1(b) shows the top view of the fabricated device with a hole 0.03 μm in diameter.

The electronic properties of the devices are measured at room temperature. The top electrode is connected to a volt-

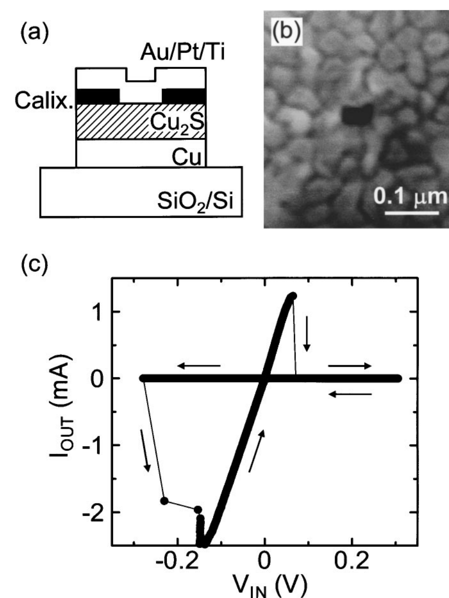

FIG. 1. (a) Schematic view of nanometer-scale switch using a Cu_2S film sandwiched between Cu film and a top electrode (Au/Pt/Ti). (b) Plane view of top electrode with a hole in the center. (c) Current–voltage characteristics of the device with a 0.03 μm hole.

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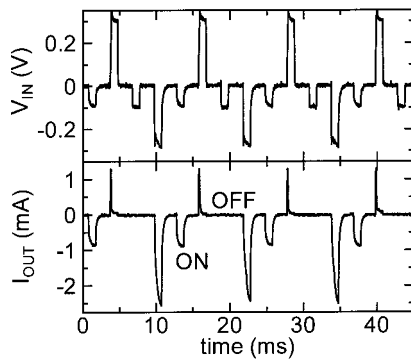

FIG. 2. Switching by applying voltage pulse for the device with a 0.03 μm diameter hole.

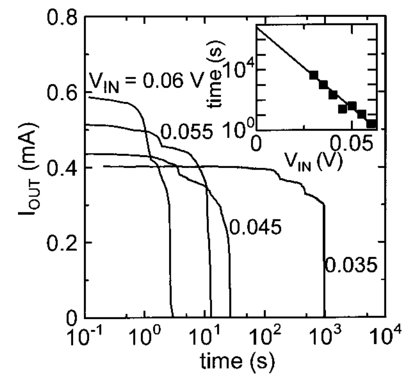

FIG. 3. Current–time characteristics showing dc-stress failure for the device with a 0.3 μm diameter hole. Different dc voltages (V_{IN}=0.06, 0.055, 0.045, and 0.035 V) are biased for each curve. Inset: Dependence of lifetime for ON state on stress voltage.

age source and the applied voltage (V_{IN}) to the electrode is monitored. The Cu electrode is grounded through the current amplifier, which monitors the output current (I_{OUT}). Figure 1(c) shows the typical $I-V$ characteristics of a device with a hole 0.03 μm in diameter. Before the voltage is biased, the conductance is very low ($<$10 nS). By sweeping V_{IN} to negative values, the conductance suddenly increases (20 mS) at -0.28 V, and an ON state of the device is achieved. As the conductance changes, V_{IN} decreases due to the voltage drops in measurement instruments and parasitic circuits. Subsequently sweeping V_{IN} back to positive values suddenly decreases the conductance at 0.066 V and the state is switched to OFF. The ON/OFF ratio is larger than 10^6. This conductance switching is repeatable, and each state persists in the low voltage regime. The ON-state conductance increases by about 10% at an ambient temperature of 77 K. This suggests that a metallic current path is involved in carrier transport. All of the fabricated devices show similar $I-V$ characteristics. The ON conductance does not depend on the hole diameter.

Switching operation of a device with a 0.03 μm hole diameter is made by biasing the pulse voltage (Fig. 2). A negative voltage pulse of -0.3 V drives the device into the ON state. The pulse width is 1 ms. The switching time is less than 100 μs and depends on the pulse amplitude. To read the state -0.1 V is applied and to switch the device to the OFF state $+0.3$ V is applied. This switching behavior is repeatedly observed up to about 3×10^3 cycles. The conductance in the ON state of each cycle varies within 10%. After about 3×10^3 cycles, the switch remains in either an ON or OFF state. This switching failure does not indicate a device degradation but a change in the threshold voltage. For the devices with a hole diameter of 0.3 μm, the cycling number is an order of 10^5. The origin of the cycling number dependence on the hole diameter is under investigation.

The dwell time in the ON state under dc stress is demonstrated using a device with a 0.3 μm hole diameter (Fig. 3). After writing operation by biasing -0.3 V pulse, constant positive voltage is applied, and the output current is monitored. For 0.06 V, the state changes to OFF after 2.5 s. For 0.035 V, the dwell time increases to 970 s. Before transitions to the OFF state, current steps are observed for each curve. The dwell time decreases exponentially as the stress voltage increases (shown in the inset of Fig. 3). When the dwell time is extrapolated to V_{IN}=0 V, the retention time without biasing the voltage is estimated to be approximately three months. In the retention time test, both states are stable without power supply for at least one month. The retention time of the devices with a 0.03 μm hole diameter cannot be estimated because the writing operation before applying dc stress is not reproducible.

Here we discuss the origin of the conductance switch. First, we rule out that a crystalline-amorphous phase transition[11] in the Cu_2S film is responsible for the switching, because the switching between the ON and OFF states depends on the polarity of the applied voltages. Moreover, electromigration of the Cu ions can be ruled out because the switching from the OFF to the ON state, where no current is observed, cannot be explained using it.

The plausible explanation for the conductance switching is the creation or annihilation of conducting paths in the Cu_2S film. We deduce that the migration of the Cu ions in the Cu_2S film results in the formation of the conducting paths.[12,13] Before applying voltages, there is no conducting path in the Cu_2S film, and the conductance is low, as discussed earlier. With applying a negative voltage to the top electrode, Cu ions migrate toward the top electrode and can be neutralized by electrons flowing from the electrode. Precipitated Cu in the Cu_2S film can form conducting paths between the Cu and the electrodes. The paths can explain the observed electrical characteristics of metals such as the linear $I-V$ characteristics and a negative temperature coefficient of conductance. On the other hand, by applying a positive voltage to the electrode the Cu can be ionized and dissolved into the Cu_2S film. The current steps under the dc stress voltage shown in Fig. 3 can be explained by the annihilation of each of the paths. The Cu electrode plays an important role because the switching is not observed when the electrode is replaced by a Pt electrode. The Cu electrode can supply the Cu ions to the Cu_2S film.

We have demonstrated that conductance switch in the sandwiched structure of a Cu/Cu_2S/top electrode can be controlled by applying low voltages ($<$0.3 V). The switching can be explained by the creation and annihilation of a conducting path inside the Cu_2S film. The device size can be scaled down to a nanometer regime, where Si microelectronics cannot be made. Our devices are advantageous for nonvolatile memory elements due to their simple structure, scalability, and low voltage operations.

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