# Nonvolatile Memory with Multilevel Switching: A Basic Model

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There is a current upsurge in research on nonvolatile two-terminal resistance random access memory (RRAM) for next generation electronic applications. The RRAM is composed of a simple sandwich of a semiconductor with two metal electrodes. We introduce here an initial model for RRAM with the assumption that the semiconducting part has a nonpercolating domain structure. We solve the model using numerical simulations and the basic carrier transfer mechanism is unveiled in detail. Our model captures three key features observed in experiments: multilevel switchability of the resistance, its memory retention, and hysteretic behavior in the current-voltage curve.

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The global proliferation of portable mobile communications is heavily reliant on the development of good high-density, high-speed, and low-power memory devices. Nonvolatile memory (NVM) is a highly promising candidate in this regard due to its drastically reduced power consumption. Among such devices, the two-terminal nonmagnetic NVM, comprising a semiconductor sandwich structure with metallic electrodes and requiring relatively few mask layers for fabrication, is potentially ideal since its size can be made arbitrarily small. The key feature of the two-terminal nonmagnetic NVM is the ability to switch the resistance of the system simply by applying a voltage or current pulse. The resistance of the device is then measured by a small bias voltage which does not perturb the state significantly, and, if the system is disconnected from the electric circuit, the resistance can remain stable. In the past few years, several novel two-terminal NVMs have emerged in rapid succession, resurrecting a field, namely, that of ovonic unified memory (OUM) [1], that has remained relatively dormant for almost 40 years. OUM utilizes the electric-pulse-driven transformation between the poorly conductive amorphous state and the highly conductive crystalline state of ternary alloys. However, these newcomers to the two-terminal NVM family seem to possess different mechanisms for their bistable resistance switching. While in one of the newcomers, $Ag_2S/Ag$ and $Cu_2S/Cu$ NVM [2], this transformation can be attributed to the migration/dissolution of Ag(Cu) ions by electric pulses, i.e., the kind of filament formation previously seen in OUM, in others, qualitatively different microscopic mechanisms are believed to be at work. The organic NVM with distributed cores of metal clusters [3], the porous Si NVM with Si nanocrystallite sites [4], the perovskite Ti and/or Zr oxides with doped charges [5–8], and the perovskite Mn oxides [9–14] are typical examples, exhibiting sufficiently fast switching capability, very low write energy with long endurance, and no wear-out properties. Collectively, they are referred to as resistance random access memory (RRAM). The most fundamental issue in current RRAM technology is the different hysteretic behavior observed in the current-voltage characteristics of different RRAM systems. Possible mechanisms for this hysteresis have been discussed phenomenologically from two broad standpoints. One assumes that the transport is dominated by some kind of charge trap in the bulk that somehow regulates the current. The other assumes a change in the contact resistance at the metal-semiconductor interface. However, no theoretical calculation has so far been performed. It is clear that for a comprehensive understanding of these phenomena, it is necessary to propose a springboard for further discussion; i.e., a basic model with several controlling parameters corresponding to each of the relevant mechanisms, e.g., the charge traps, the interface barriers, and so on.

We present here a theoretical model which attempts to meet the above requirements. Our results show a remarkable qualitative agreement with several essential RRAM behaviors, namely, hysteresis, resistance switch, and retention.

Some features of the model are motivated by rather universal aspects of strongly correlated perovskites such as the doping-induced insulator to metal transition and the spatial inhomogeneity (or phase separation) that occurs at the nanoscale [15,16]. Thus, the model assumes an insulating (and inert) medium sandwiched by two metal electrodes. The insulating medium contains nonpercolating metallic domains, which inexplicitly correspond to charge traps in the real system such as dopants, vacancies, metallic clusters, nanodomains, and so on. We assume that there are just three types of domain, schematically depicted in Fig. 1. The top and bottom domains are taken to be smaller than the middle one. This differentiation might be justified by the different electronic states around the interface at the metal electrodes.

  

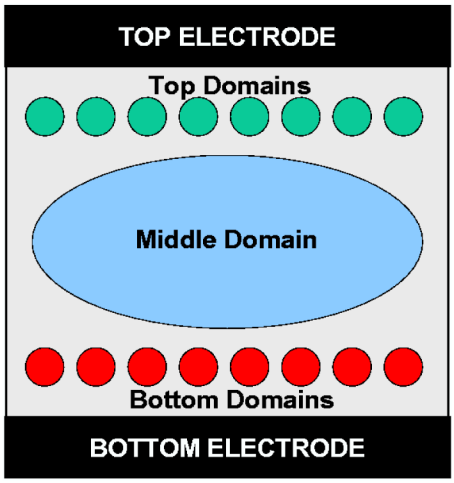


FIG. 1 (color online). Schematic view of the model with top and bottom electrodes, insulating medium, smaller top and bottom domains, and large middle domains. In this work we set $\Gamma_{ET} = \Gamma_{EB} = 0.4 \times 10^{-16}$ and $\Gamma_{TM} = \Gamma_{BM} = 0.3 \times 10^{-11}$, the number of top and bottom domains to 40, and the number of states that they hold to $10^6$; the sole middle domain holds $10^8$ states.

The carriers are assumed to occupy domains or electrodes at all times. They move around by hopping between domains as well as between a domain and an electrode, only when there is an external voltage (potential difference), i.e., the drift current is neglected. The number of states that the domains can hold is simply assumed to be proportional to their physical size. The model is further characterized by the domain-domain and domain-electrode tunneling rates and the number of domains of each type. The tunneling rate physically corresponds to the overlap of the carrier wave functions. To make the model more realistic, we adopt random tunneling rates $\gamma_{AB}$ drawn from a uniform distribution with mean value and width $\Gamma_{AB}$, where $A$ and $B$ denote two domains and/or electrodes.

We solve the model by Monte Carlo simulations of carrier transport. The transition probabilities for transferring a carrier from $A$ to $B$ is given by an expression resembling Fermi's golden rule

$$p_{AB} = \gamma_{AB} N_B [1 - n(B)] f_{AB}(V), \quad (1)$$

where $n(B)$ is the occupation of $B$ and $N_B$ is the total number of states of $B$. The function $f_{AB}(V)$ reflects the dependence of the transition probabilities on the applied external voltage $V$. The precise functional form, which is very difficult to compute, depends on the specifics of the individual devices [17]. For definiteness and simplicity, we adopt a rather natural, exponential form for $f_{AB}(V)$. Our convention is that positive $V$ moves carriers from the bottom electrode into the bottom domains and out of the top domains into the top electrode. It should be noted that we take $f_{AB}(0) = 0$. This means there is no current when there is no applied voltage, because both the drift current and the internal relaxation current are expected to be very small. We shall return to this point later. The actual number of carriers of domain-domain transfer or domain-electrode transfer is assumed to follow from a Poisson process.

We make the natural assumption that the interdomain tunneling amplitudes are much larger than the electrode-domain ones [18]. Thus, there are four phenomenological tunneling amplitudes: $\Gamma_{ET}$, $\Gamma_{EB}$, $\Gamma_{TM}$, and $\Gamma_{BM}$, which correspond to tunneling between electrode–top, electrode–bottom, top–middle, and bottom–middle, respectively.

As it stands, this RRAM model assumes that the main conduction mechanisms are through charge injection and tunneling. The limited number of states that a domain can hold renders it impossible for carriers to hop further into an already fully occupied domain. This mimics the space-charge-limited conduction effect that is relevant at high fields [19]. Furthermore, the combination of $\Gamma_{ET}$, $\Gamma_{EB}$, and the occupation number of the small top and bottom domains somehow emulates the interface behavior. For the sake of simplicity, in this initial study, we focus on a symmetric case taking $\Gamma_{ET} = \Gamma_{EB}$ and $\Gamma_{TM} = \Gamma_{BM}$.

We now turn to a discussion of the results. The basic switching behavior of the model is demonstrated in Fig. 2. An external direct-current (dc) voltage bias $V_{read}$ is continuously applied between the top and bottom electrodes and produces a carrier current. At given time intervals of 1000 uot [20], voltage pulses of short duration (10 uot) are applied. The positive voltage pulses cause sharp positive current spikes, while the negative pulses cause negative spikes. The middle panel shows the same quantity in a different vertical scale that reveals more detailed behavior between the pulses in the presence of a small dc bias $V_{read}$. The most important point to note is that voltage pulses switch the system between two conductance (or resistance) states corresponding to high and low current [21]. The bottom panel shows the resistance $R \propto 1/I$ at constant $V$, demonstrating that the system switches reversibly between two well defined resistance states, more than an order of magnitude apart. The high-$R$ state can be assimilated to a logic "1" and the low-$R$ to a logic "0." It is interesting to note that the system starts in an arbitrary initial state (assumed for simplicity with all domains half-filled) thus having an arbitrary $R$. The action of a write pulse does not properly switch the system to "1," and only after an erase pulse is applied does the system get properly initialized and begins switching between well defined $R$ states [22]. This behavior is qualitatively observed in a variety of real RRAM systems [3,6,11,14]. We show in Fig. 2(b) similar results, but for a different protocol of applied pulses. In this case, five consecutive write pulses are applied, followed by three erase pulses, and so on. A striking feature of the model emerges in that each successive write pulse switches the system to a

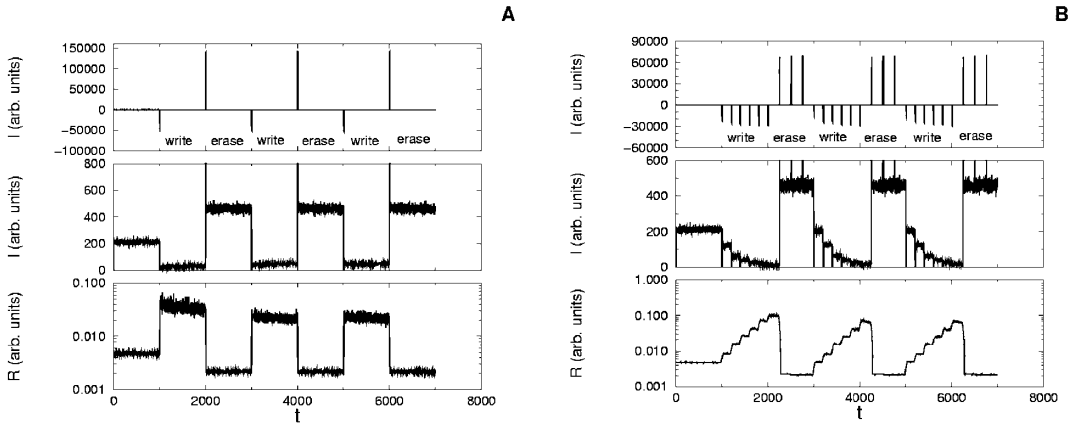


FIG. 2. (a) Top panel: Electrode current as a function of simulation time. The pulses have a duration of 10 uot. Positive pulses erase and negative pulses write. Middle panel: Idem as the top panel in an enlarged $y$-axis scale. Bottom panel: Resistance ($\propto 1/I$) as a function of simulation time. (b) Idem as (a) but for the multilevel switching protocol.

different $R$ state, while a single erase pulse is sufficient to switch back to the original state. Thus, a multilevel memory effect is captured by the model. This is qualitatively similar to the perovskite (Ti-, Zr-, and Mn-) oxide-based RRAMs [6,7,11,13].

To gain more insight into the behavior of the model, it is useful to look at the occupation of the domains during the simulation of an applied $V(t)$ protocol. These quantities are shown in Fig. 3 for a similar protocol as in Fig. 2. Upon application of a pulse, a large carrier transfer occurs over a very short time period. The occupation of the top and bottom domains is significantly changed due to a large carrier transfer in and out of the large middle

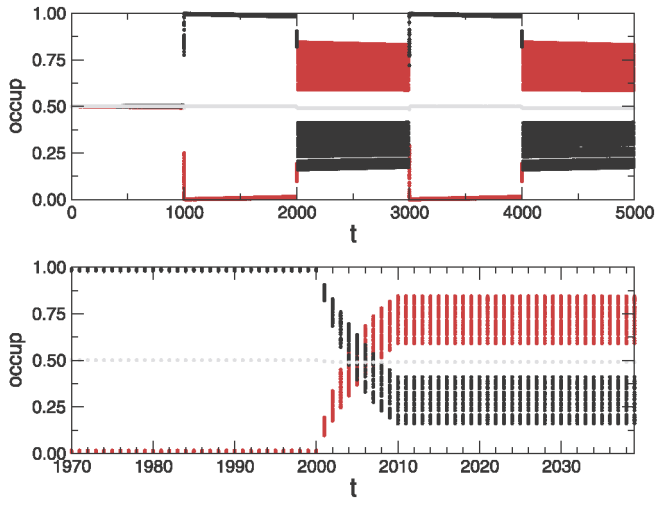


FIG. 3 (color online). Top panel: Domain occupation as a function of simulation time. Top domains are in black and bottom domains are in gray. The middle domain occupation remains close to 0.5 (light gray). Note that the occupation of top and bottom saturates after the erase pulse, but not after the write one. Bottom panel: Idem to the top panel in an enlarged $x$-axis scale that highlights the rapid decharging and charging of the top and bottom domains during the pulse application.

domain. The new occupation state of the top and bottom domains is reflected in a qualitative change in the read current. A write (negative) $V$ pulse fills up the bottom domains and empties the top ones. While $V_{\text{read}}$ is continuously applied, the systems remain in a high-$R$ (low-$I$) state, since the probability of carrier transfer into the already filled bottom domains is low and likewise, the probability of carrier transfer out of the emptied top domains to the electrode is also low. On the other hand, an erase (positive) pulse produces a large transfer from the middle to the top domain and from the bottom to the middle domain with concomitant changes in the occupations. The result is that, under the applied $V_{\text{read}}$, the systems now displays a low-$R$ (high-$I$) state as carriers can be easily transferred to the empty bottom domains from the bottom electrode and from the fully filled top domains to the top electrode.

The variation in the carrier number distribution discussed above is suggestive of a diode with its polarity reversed by the applied pulse. This is indeed reflected in the hysteretic behavior of the current-voltage ($I$-$V$) curve. We have investigated the $I$-$V$ hysteresis by application of a sawtoothlike $V(t)$. In Fig. 4 we show the resulting $I$-$V$ characteristic. Negative $V$ corresponds to negative $I$, but we plot the absolute value $|I|$ in order to facilitate the use of a semilog scale. The hysteretic behavior can be clearly observed [23]. This behavior is qualitatively similar to that observed in the organic RRAM system [3] and perovskite (Ti- and Zr-oxide-based) RRAMs as well [5,8]. However, other effects are reported as well that do not seem to be captured by the model and might call for further extensions and fine-tuning [4,6–8,12,14].

Finally, we briefly address the issue of nonvolatility. The current at the electrodes is essentially given by the charging or decharging of the top and bottom domains. However, the largest carrier transfers occur between those domains and the middle one, since the interdomain tunneling amplitudes are higher. The read currents (i.e.,

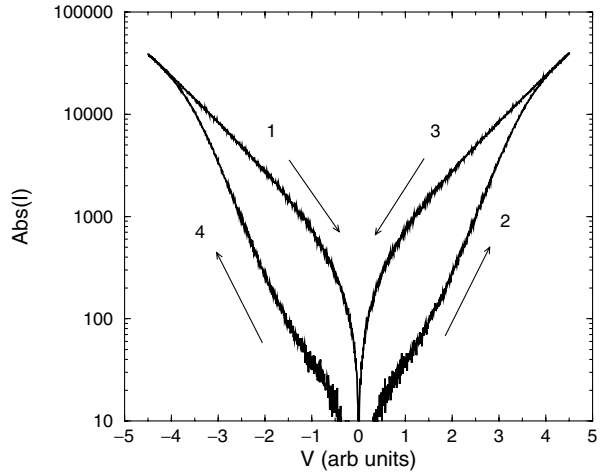


FIG. 4. *I-V* characteristic showing an hysteresis cycle. The voltage protocol corresponds to a positive ramp from $V = -4.5$ to $V = 4.5$ during a time interval of 1500 uot (paths 1 and 2) and ramp back to $V = -4.5$ (paths 3 and 4).

when $V_{\text{read}}$ is applied) are small so they change only the occupation of the top and bottom domains very slowly. Thus, the logic states are able to remain well defined for long reading times. In real systems, the depolarization effect due to the inverse *internal* bias arising from the inhomogeneous charge distribution must also be taken into account. For the particular domain structures considered in our model and using realistic values for the carrier density, dielectric constant, and thickness [24], we have estimated that the inverse voltage is at most one order of magnitude smaller than $V_{\text{read}}$ used in experiments. One may therefore expect the concomitant depolarization currents (leakage currents) to be substantially smaller than the reading currents. These features are consistent with the experimentally observed nonvolatility effect, namely, if disconnected the device remains in a given memory state for months.

In summary, we have presented a phenomenological model that captures many qualitative features observed in a variety of RRAM systems. Though simple, this model might provide useful guidance in this active and promising area of research. Many interesting questions remain for future theoretical consideration such as what features strong correlation effects (e.g., Coulomb blockade effects or Mott transitions [25]) can add to the behavior of the systems. Moreover, by taking into account magnetic degrees of freedom, we may open up even more exciting possibilities, especially in the perovskite Mn-oxide RRAMs.

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[20] 1 uot = 1 unit of time = 1 Monte Carlo step in which all domains are updated.
[21] The noise in the current is due to the Poisson nature of the carrier transfer process, yielding current fluctuations that are similar to those experimentally observed.
[22] We assume the positive (erase) voltage pulses to be 20% larger than the negative (write) ones. Thus, the occupations (Fig. 3) saturate only upon erase.
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